Characterize the high-speed data path from the computer to the display.

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Characterize Digital Display Interfaces

With the performance gains of each new computer generation comes an increase in the size of the display. To manage these ever-larger displays, the graphics system must control an ever-increasing number of pixels. The number of pixels in a 640×480 VGA display is only 307,200. However, to operate the 2048×1536 QXGA display, the graphics system must control 3,145,728 pixels.

The majority of monitors use tubes, which require analog signals to drive them. Although LCDs are digital, they are often driven with analog signals for compatibility. Even so, the LCD is purely digital inside, and the analog technology inside the PC will disappear as LCDs replace the older tube technology. The industry has already created several standards that enhance or replace the good old 15-pin-wide analog VGA interface:

- P&D (Plug and Display Port)
- DFP (Digital Flat Panel Port)
- DVI (Digital Visual Interface)

Common to all of these standards is that the display data coming from the graphical controller on several parallel lines is transmitted digitally. The color and control information is serialized onto a few high-speed lines. These lines run on low-voltage differential signaling (LVDS) technology, which provides several advantages:

- High bandwidth that is mostly independent of connection length
- Low emission and high noise immunity
- Good system integration capability
- Reasonable power consumption
- Cheap cable and interconnection technology

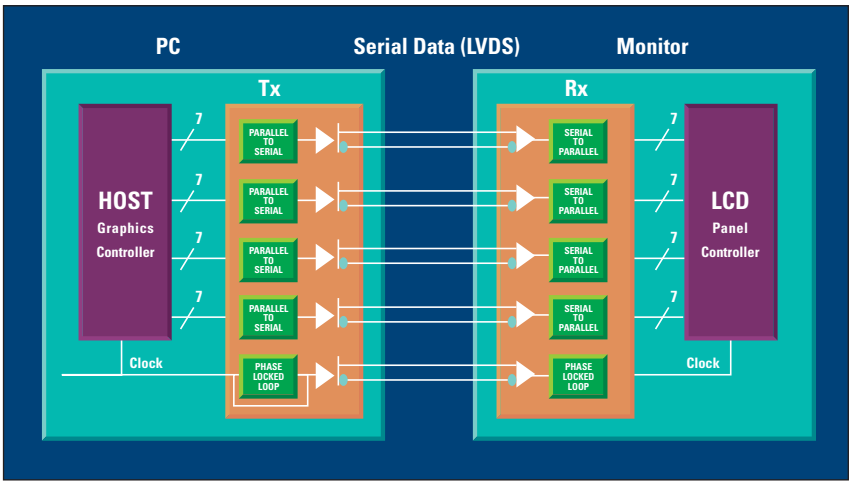


Figure 1. A typical digital display interface.

DVI is capable of handling QXGA with a resolution of 2048×1536 pixels, which requires a data rate of up to 1.8 Gb/s. The DVI standard proposes to double the channels for transmitting the color information by using dual transition-minimized differential signaling (TDMS) channels for each color. Doubling the number of transmission lines reduces the data rate on each line. The TDMS method also minimizes the average frequency and balances the signals DC-wise. However, practical implementations achieve and exceed QXGA performance without doubling the number of transmitting channels (so the doubled channels could be used for future pixel-rate increases).

Figure 1 shows a block diagram of a typical digital display interface. The color and control information is multiplexed/demultiplexed into four serial channels. As the multiplexing/demultiplexing factor is seven, the data rate on the serial interface is seven times higher than on the parallel side. The transmitted clock signal is the same frequency on the parallel and serial sides. The serial interface runs on LVDS technology, which generally uses a 250-mV amplitude.

Verify the Performance of the Interface

Before using any of the digital display interfaces, you must make sure that you will be able to test the performance of your implementation. The parameters to be char-

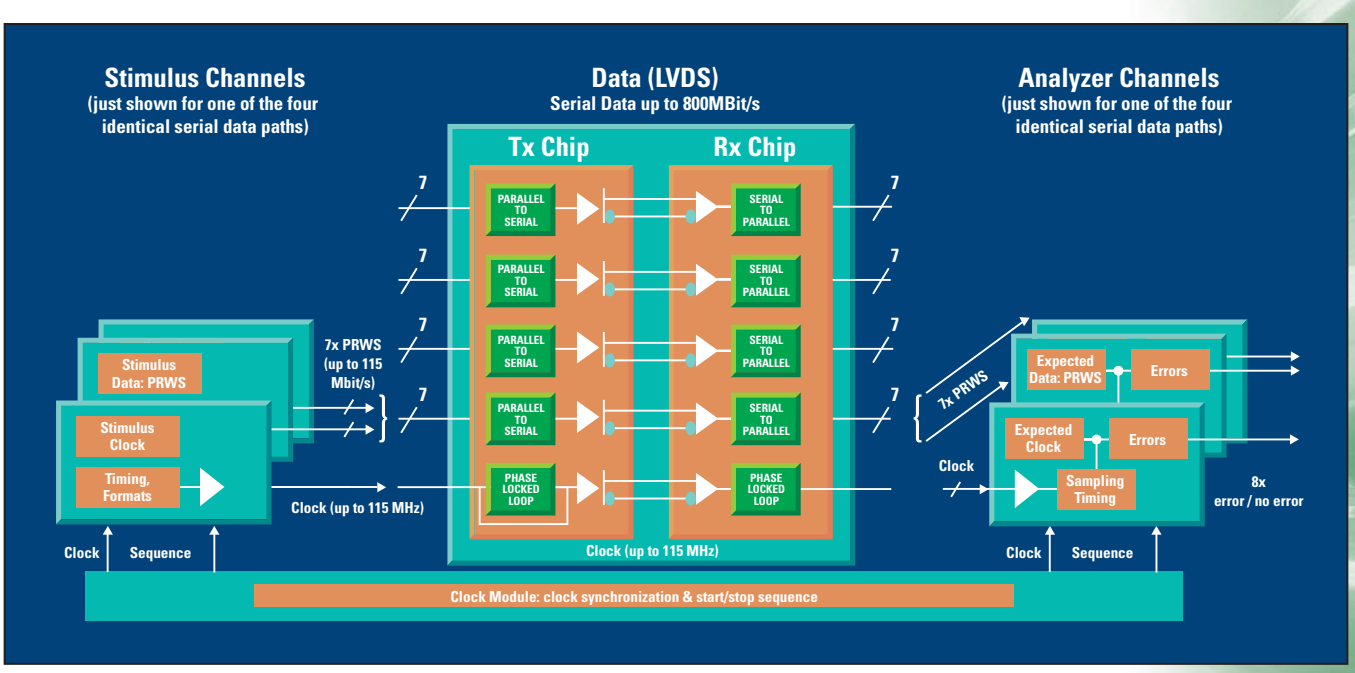


Figure 2. The test setup for testing a full display interface.

acterized for the display interface can be considered separately for the complete link consisting of the transmitter, interconnection, and receiver, and for the individual transmitter (TX) and receiver (RX) chips.

For the complete link, the characteristics to consider (beyond regular functionality) are:

- What is the maximum operating clock rate and data transfer rate?
- How does the interconnect length affect performance? (Is the bandwidth sufficient, and are losses to be neglected?)
- How does EMI and electromagnetic field strength affect performance?
- What radiation level is reached?

For the individual chips, the questions are:

- What are the timing relations (setup/hold times, propagation delay times) of the input and output data and control signals in reference to clock?
- What is the maximum operating speed, and is it dependent on other parameters?
- How are timing relations affected by data content (jitter)?
- How are the timing relations correlated to variations of power supply voltage and ambient temperature?

The timing relations between input and output signals are more complex than usual as the data rate being transmitted along the serial link is not the same as the data rate arriving at the TX chip. Also, the serial data from the multiplexers must be synchronized to parallel data going into the TX chip.

The RX chip points to consider are:

- Window of correct sampling of input data in reference to input clock
- Parallel data out to clock out (setup/hold provided)
- Jitter
- Maximum operating frequency

On the TX chip the timing relations of interest are:

- Parallel data in to clock (setup/hold sensitivity)

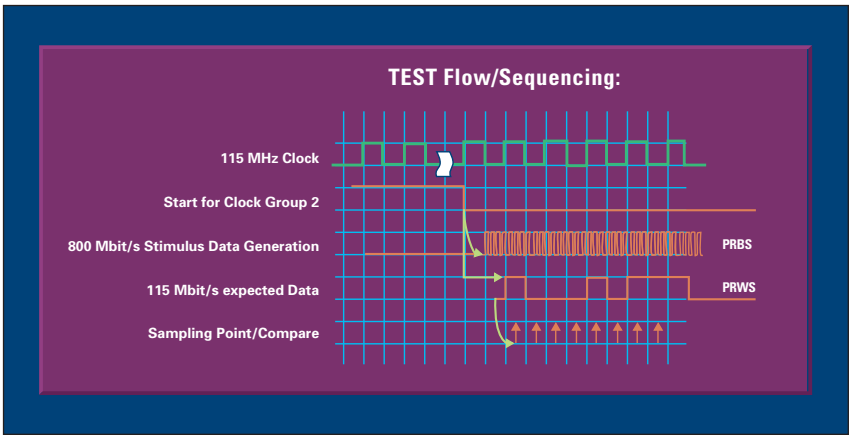


Figure 3. The signal flow for testing the RX chip.

- Serial data out to clock (propagation delay with proper phasing)
- Serial data to clock out (setup/hold provided)

The test setup for the complete link is shown in **Figure 2.** A set of data generator channels sends data and clock to the parallel inputs of the TX chip. The TX and RX chips are similar for all four serial channels, so it is sufficient to deal with one of the serial channels at a time. In production it would be necessary to test all of the paths at the same time to reduce test time.

Check Gathered Data Against Expected Data

The output of the RX chip is connected to the analyzer input channels. This data is then checked against the expected data, a process called Real-Time Compare. If the incoming data is different than expected, the analyzer reports the errors immediately as well as at the end of the test run. Stimulus and analyzer channels of the test system run synchronously; a central resource of the test system provides clock and start/stop information to every channel. The latency from TX chip input to RX chip output must be adjusted for by delaying the sampling of incoming data within the analyzer channels.

It is important to choose appropriate data for the test. The communications industry has developed a pseudo-random binary sequence (PRBS) that allows you to define the stress placed on the system from cycle-to-cycle data changes and from intervals with a maximum length of consecutive ones and zeros. The data applied to the parallel side of the TX chip as a pseudo-random word sequence (PRWS) will be such that the PRBS sequence will be obtained on its serial side. The same PRWS can be used as the expected data for the analyzers. This setup allows the maximum clock/pixel rate to be evaluated.

Another issue in evaluating the maximum data rate for the device under test (DUT) is the error rate. Classically, the maximum speed would be the speed that produces no errors; any single bit error would be treated as a failure. However, in this case it is appropriate to evaluate noise immunity in terms of bit error rates. The DUT is allowed to fail for a specified amount of transferred data. Within the communications industry it is a common practice to test against certain bit error rates, but this requires careful designs including error-correcting circuitry. For a display interface, error correction is not necessary as the human eye can readily tolerate single pixel failures appearing on a display.

Real-World Stress

It is important that test vectors such as PRBS/PRWS apply stress during the test similar to what the DUT would encounter in its application. As long as the test system provides for doing the characterization by evaluating the bit error rate, the designer can define the error limit to be either zero or any finite number depending on the nature of the test. This kind of testing is called Parallel Bit Error Analysis.

Because the test system handles the different speeds at the input and output of the chip, the input is stimulated seven times faster than the output is analyzed. The PRBS provides the stimulus and the analyzer can use the PRWS as the expected data. The different frequencies used for stimulation and analysis need two clock groups on the test system. The generator runs at up to 800 Mbit/s, while the

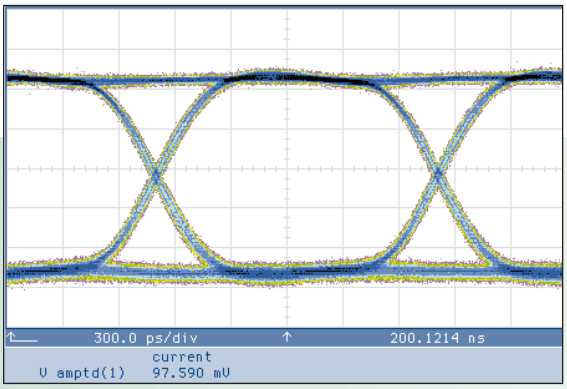
analyzer compares at up to 115 Mbit/s. For synchronization between the two clock groups, the generator feeds two signals to the analyzer part: Clock and Start. These are in addition to the stimulus signals running to the DUT. **Figure 3** shows the signal flow for testing the RX chip.

To obtain synchronous data analysis, the generator sequencing must provide a test start according to the Test Flow diagram: the clock starts to get the device's PLL and the Analyzer Clock Group working. When they are settled, the Start signal initializes the generation of expected data. This must occur prior to generation of stimulus data to compensate for analyzer latency. When this is completed, the stimulus PRBS data is applied and the comparison with the PRWS in the analyzer can take place. Programming the sampling point delay compensates for the latency through the DUT.

The use of two clock groups is not mandatory. The device could also be tested using the same high-speed clock at the low-speed parallel outputs. This would result in oversampling the outputs by a factor of seven. However, you would lose the automatic generation of the PRWS test vectors; obtaining test vectors would require a manual approach such as gathering the bits from a golden device.

There are times when the device being tested must operate at a speed that is beyond the basic rate of the test system. For example, the HP 81200 has a front-end bandwidth of 660 MHz. To test at rates higher than 660 MHz, the channel-add feature must be used to combine the digital resources from two channels. The channel-add feature allows you to analyze a system with data rates up to 1.3 Gb/s.

With the setup described in this article, all characterization measurements regarding the target can be obtained. This requires timing variations of the various signals, which can be done manually or by program control. The most effective method is for the test system to provide high-level software functions that can do the timing variations automatically and provide appropriate graphical representation.



Analyze High-Speed Differential Signals

The low-voltage differential signals now being used for high-speed data transfer require the appropriate tools to handle the differential nature of the signals along with the high data rates. Two new front ends for the HP 81200 data generator/analyzer provide the capabilities to work with the latest high-speed differential technologies. The 660-MHz HP E4837A Differential Analyzer Front-End along with the E4838A allow you to characterize and verify the operation of differential technologies such as LVDS (Low Voltage Differential Signaling), ECL (Emitter Coupled Logic), and PECL (Positive-biased Emitter Coupled Logic). The generator has an amplitude range of less than 0.1 to 3.50 Vpp, and a resolution of 10 mV.

The HP E4838A 660-MHz Variable Slope Generator Front-End can adapt to other technologies such as CMOS and TTL. It has variable transition times of 0.5 ns to 4.5 ns at both edges at the same time. The output level can be set up to 3.5 Vpp from 50 Ω into 50 Ω. The variable transition time also allows you to conduct transition-time-dependent measurements such as crosstalk versus transition time.

The HP 81200 provides real-time stimulus and response capabilities in a single instrument. It helps you to characterize and verify digital subsystems, ICs, and boards for computer and telecommunications products. Its configurable nature allows it to easily adapt to the measurement task at hand.

For more information, check 4 on the reply card, or visit http://www.agilent.com/find/insight4.